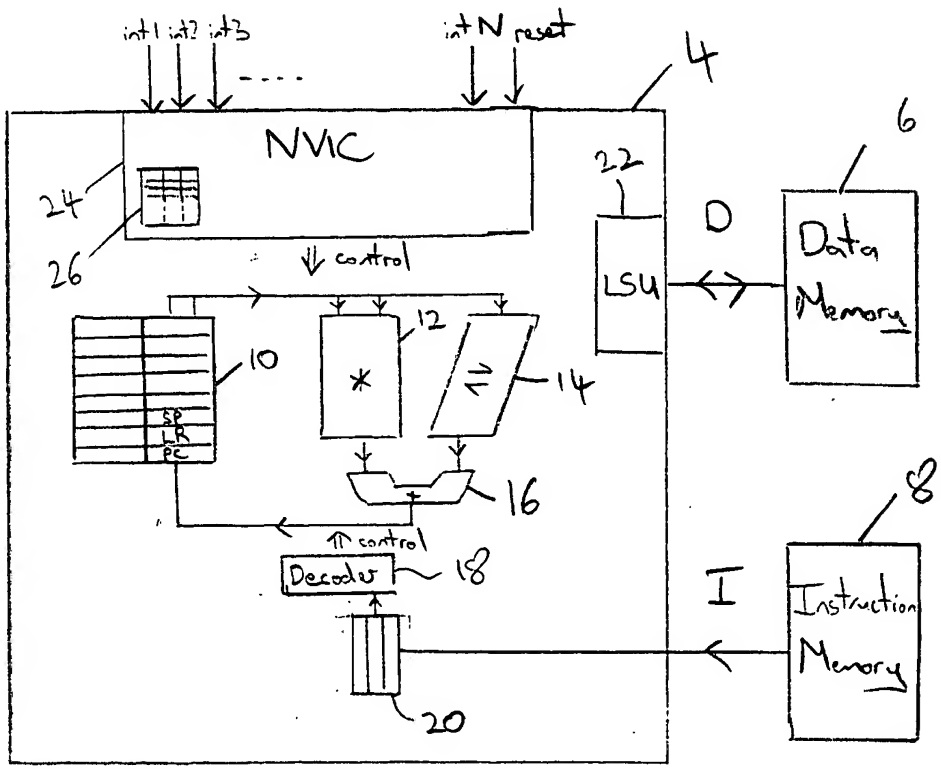

int1 int2 int3
intN reset
4
NVIC
24
26
control
22
LSU
D
6
Data Memory
10
12
14
SP
LR
PC
16
control
Decoder
18
I
8
Instruction Memory
20

Fig. 1

NVIC Control Table

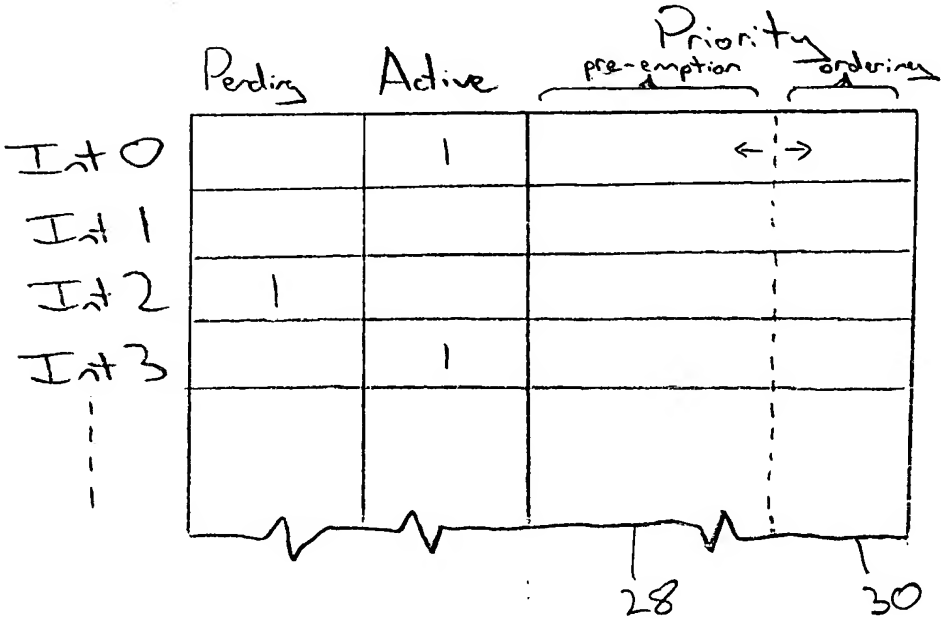
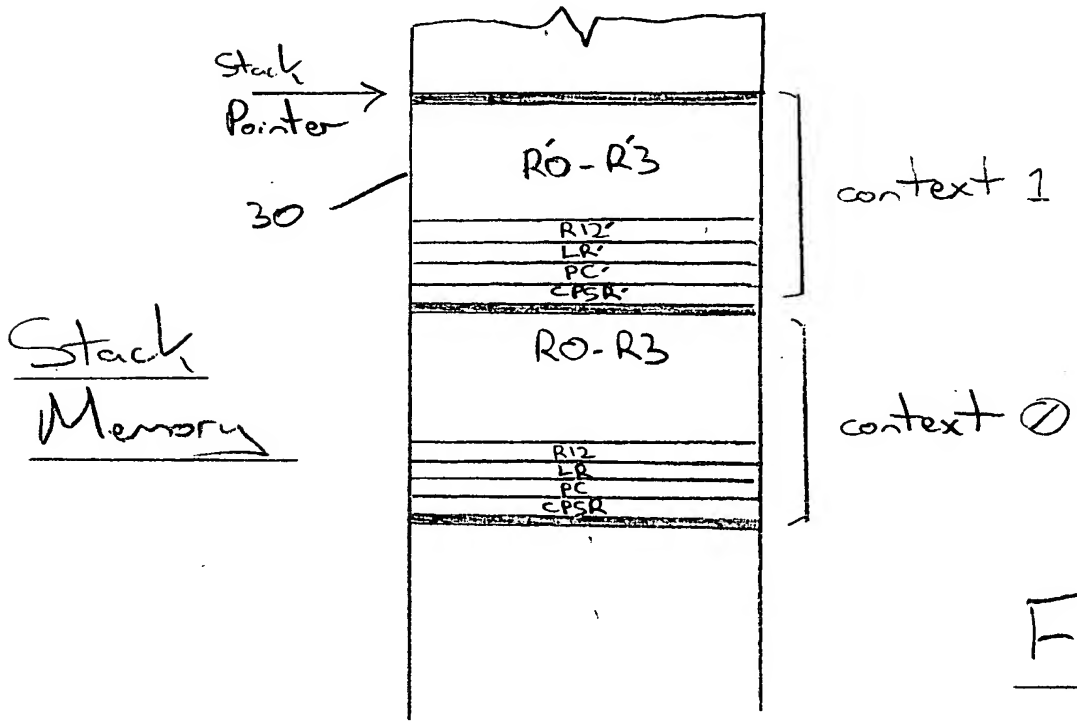


Fig. 2



Stack Memory

Fig. 3

Priority Inversions

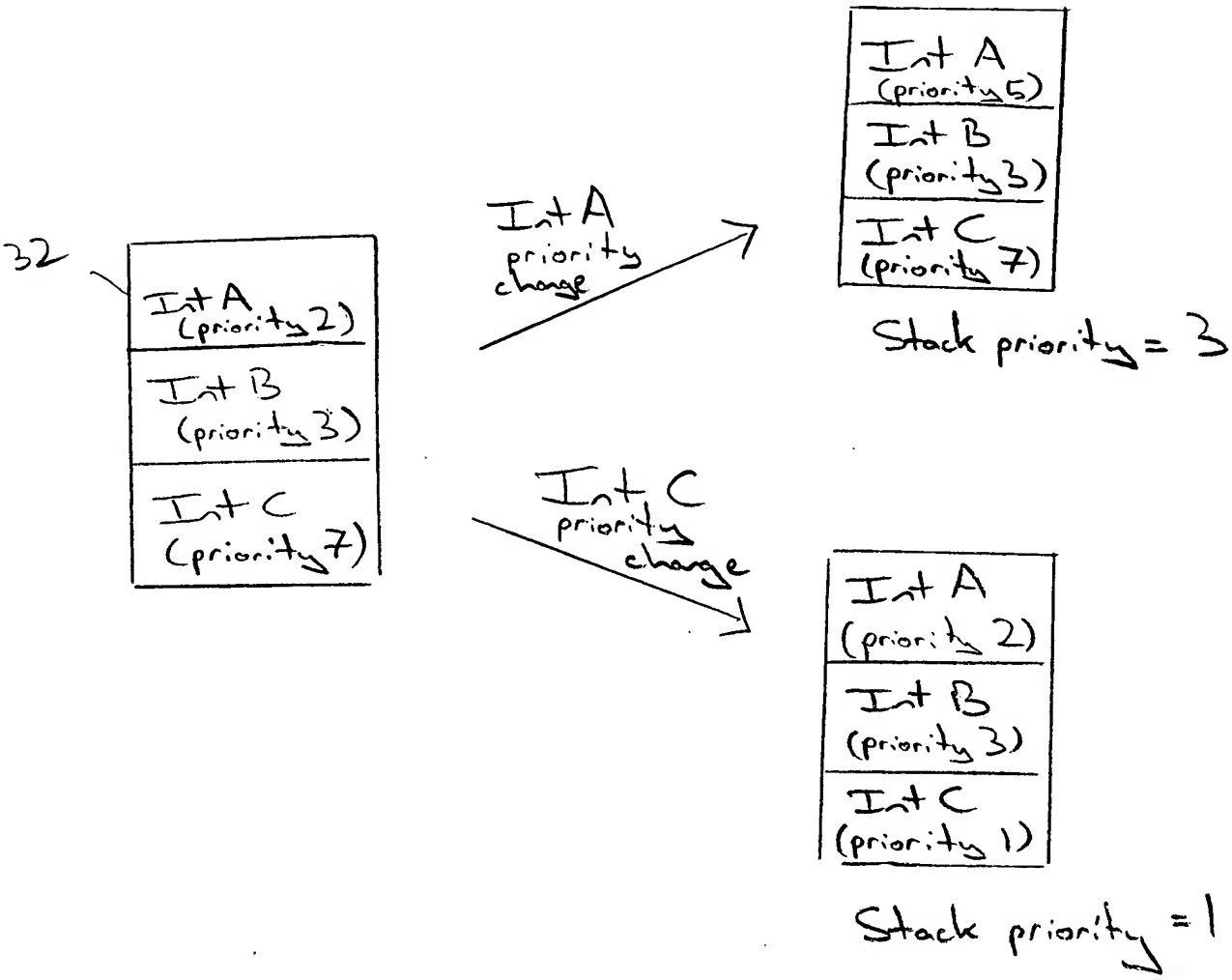


Fig. 4

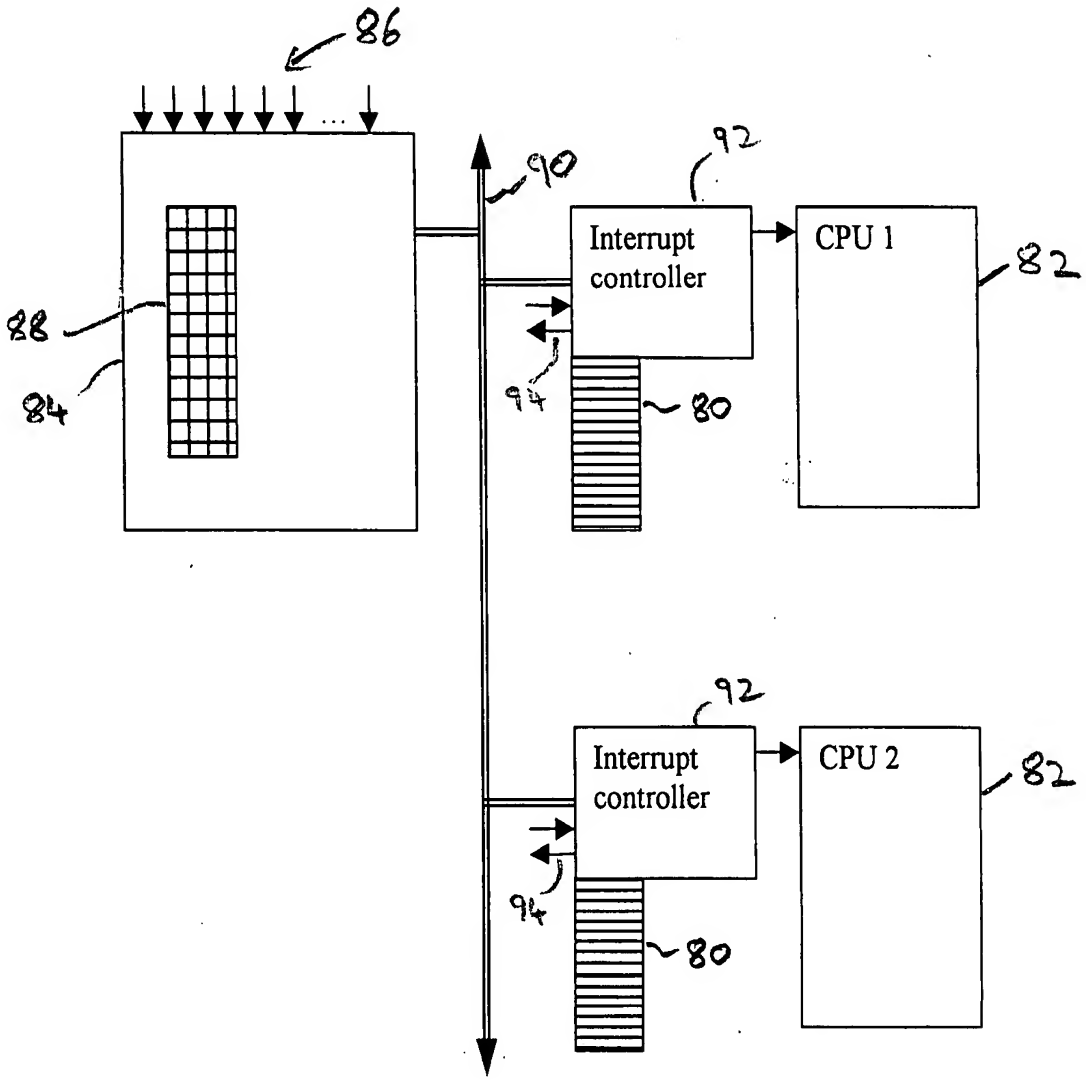

86
88
84
90
92
Interrupt controller
CPU 1
82
94
80
92
Interrupt controller
CPU 2
82
94
80

Fig. 5

Main Flow

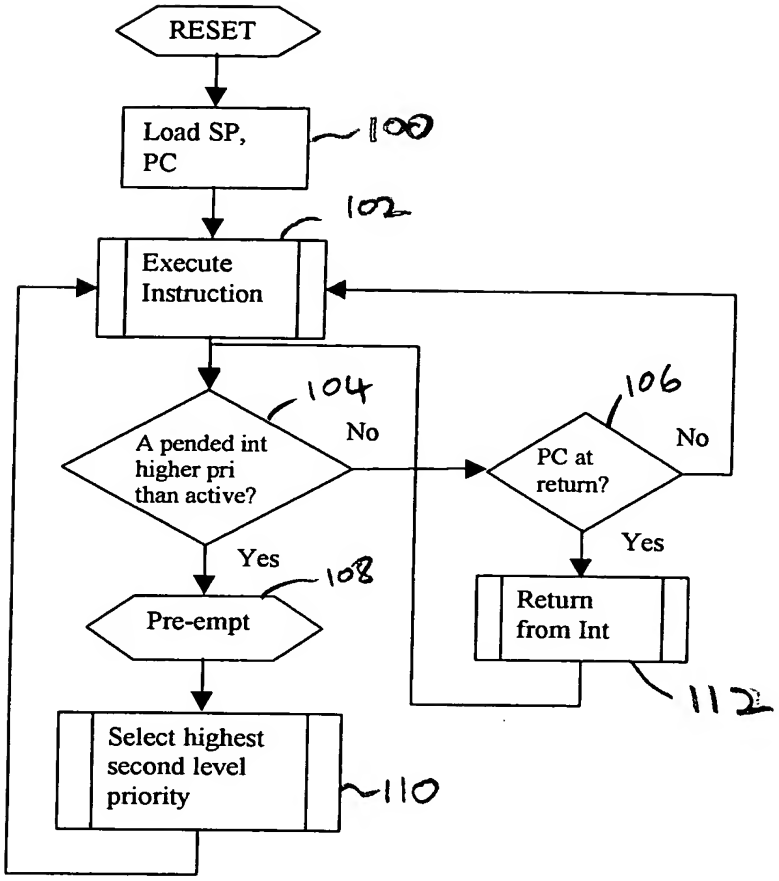


Fig. 6

Main Flow with Tail Chaining

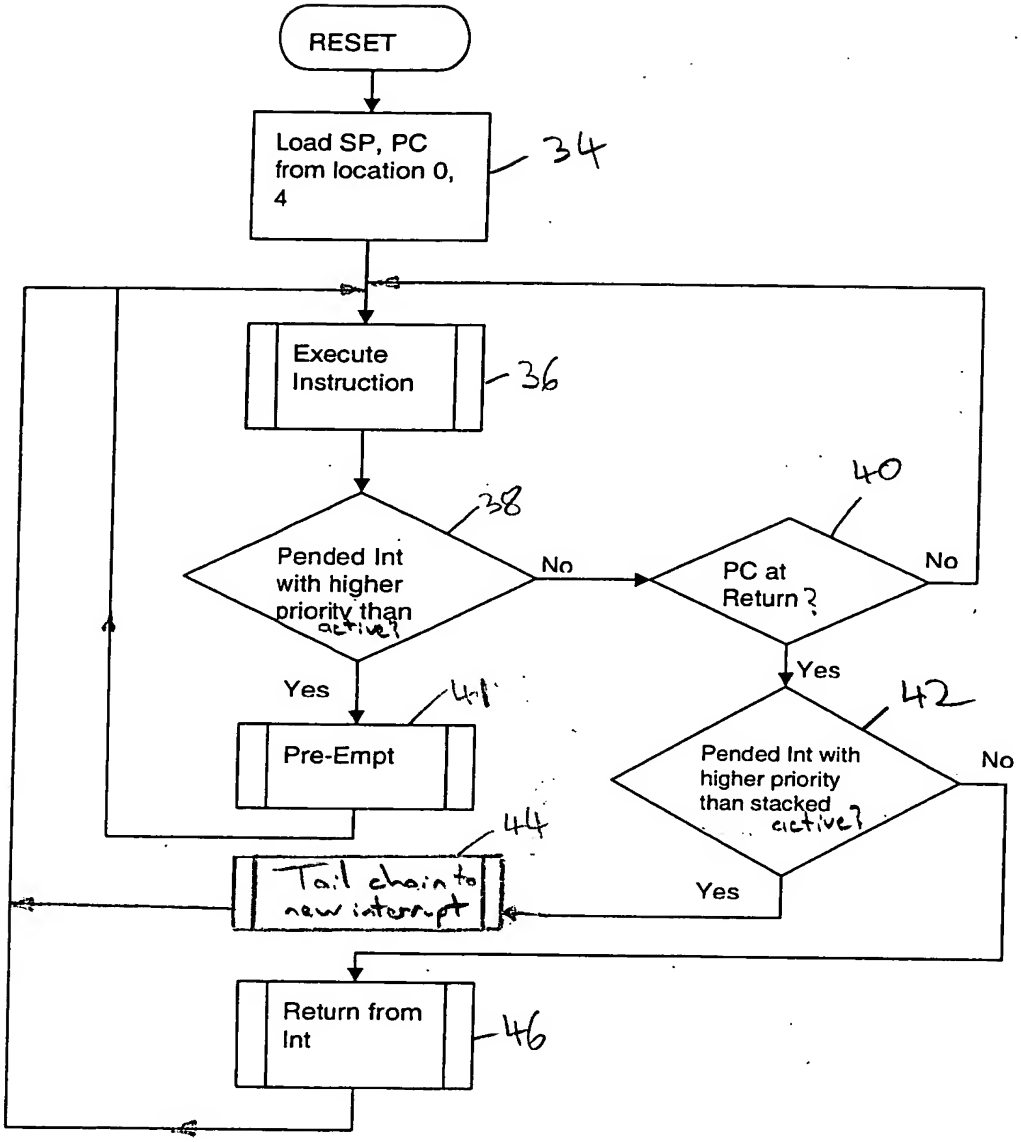


Fig. 7

Pre-emption Flow

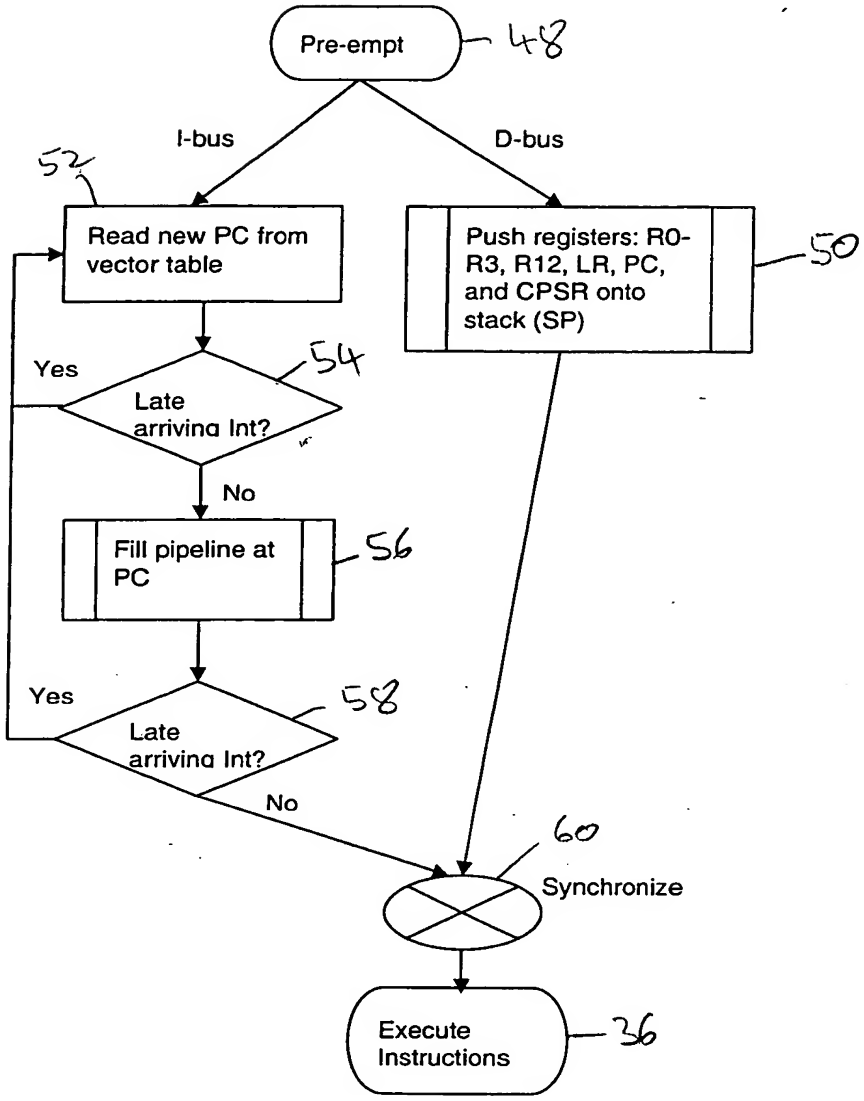


Fig. 8

Return From Interrupt Flow

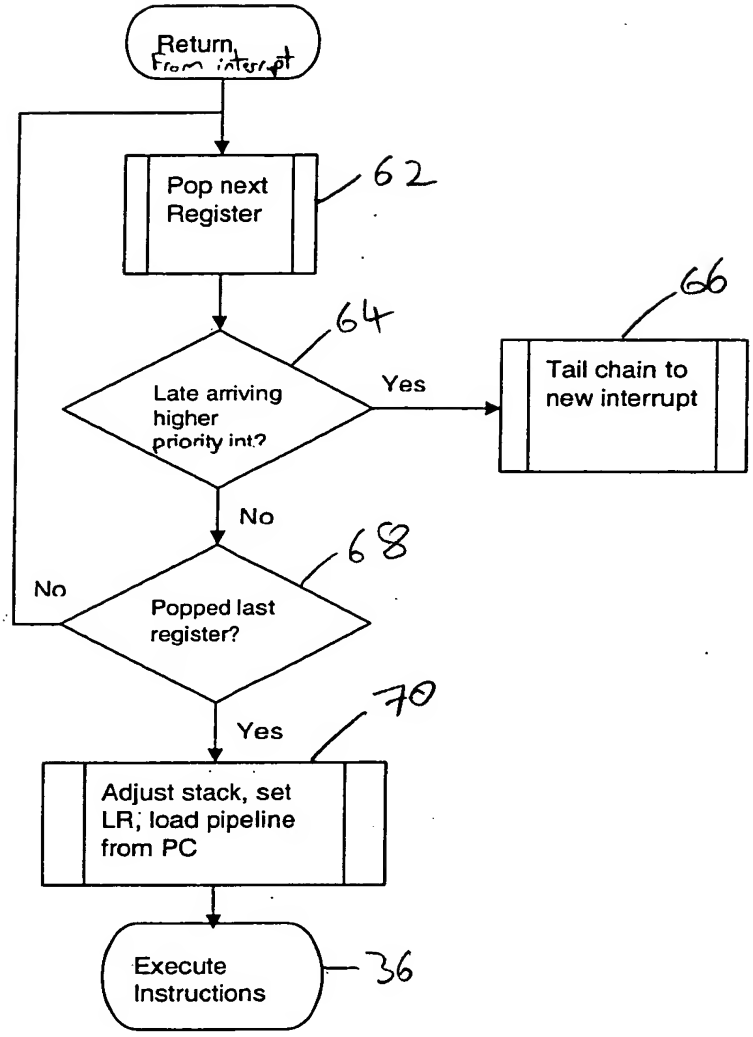


Fig. 9

Tail Chaining Flow

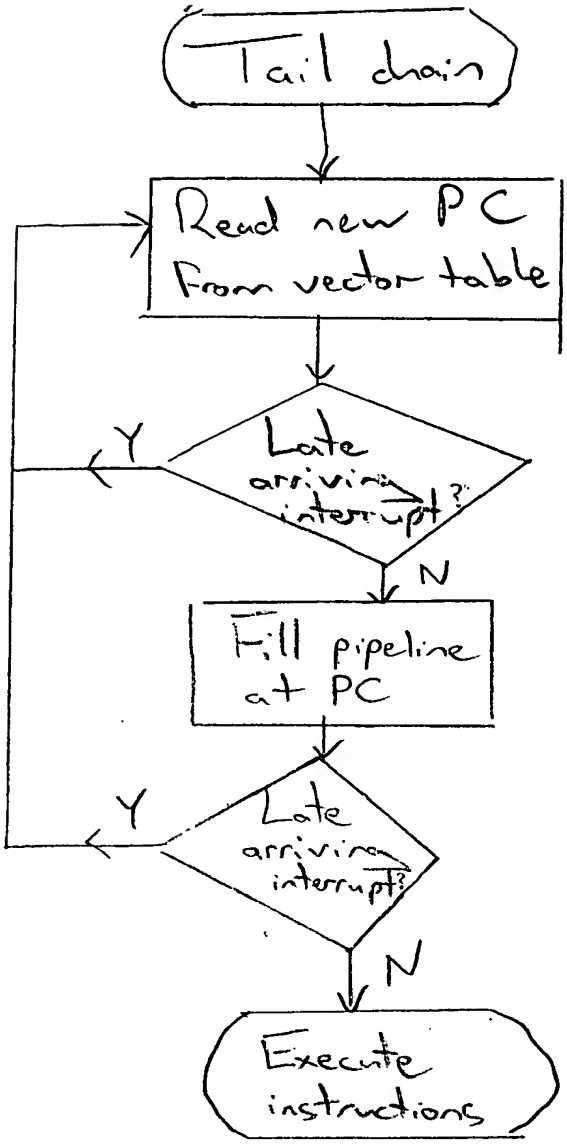


Fig. 10